What is claimed is:

Sub A1

1. A semiconductor integrated circuit device having a zener diode composed of a first semiconductor region of a second electrically conducting type formed in a primary face of a semiconductor substrate of a first electrically conducting type, and a second semiconductor region that is a first electrically conducting type that is formed in the semiconductor substrate at a bottom portion of said first semiconductor region and is smaller than said semiconductor region in an area surrounding a planar pattern thereof,

the device comprising a plurality of first connection holes for connecting said first semiconductor region and a wire to each other wherein the first connection holes are arranged in a region being outside a junction formed between said first semiconductor region and said second semiconductor region.

Sub B2

2. A semiconductor integrated circuit device according to claim 1, wherein said second semiconductor region is arranged at a substantial center of said first semiconductor region, and said plurality of first connection holes are arranged at a periphery of said first semiconductor region.

Sub C3

3. A semiconductor integrated circuit device according to claim 1, wherein a junction depth of said first semiconductor region in a region in which said first and second semiconductor regions form a junction is shallower than that of said first semiconductor region in a region in which said semiconductor substrate and said first semiconductor region form a junction.

4. A semiconductor integrated circuit device according to claim 1, wherein each of said plurality of first connection holes is spaced from each other so that a pitch between the adjacent first connection holes is greater than a minimum pitch between connection holes of the circuit.

5. A semiconductor integrated circuit device according to claim 4, wherein the pitch between said adjacent first connection holes is two times and more of the minimum pitch between the connection holes of said circuit.

6. A semiconductor integrated circuit device according to claim 5, wherein the pitch between said adjacent first connection holes is three times and more of the minimum pitch between the connection holes of said circuit.

7. A semiconductor integrated circuit device according to claim 6, wherein the pitch between said adjacent first connection holes is four times and more of the minimum pitch between the connection holes of said circuit.

Sub A2

8. A semiconductor integrated circuit device having a zener diode composed of a first semiconductor region of a second electrically conducting type formed in a primary face of a semiconductor substrate of a first electrically conducting type, and a second semiconductor region that is a first electrically conducting type and is formed in the semiconductor substrate at a bottom portion of said first semiconductor region and is smaller than said first semiconductor region in an area surrounding a planar pattern thereof,

the device comprising a plurality of first connection holes for connecting said first semiconductor region and a wire to each other wherein said first connection holes are arranged in a region being outside a junction formed between said first semiconductor region and said second semiconductor region, and wherein each of said plurality of first connection holes is spaced from each other so that a pitch between the adjacent first connection holes is greater than a maximum pitch between connection holes

of the circuit.

9. A semiconductor integrated circuit device according to claim 8, wherein a junction depth of said first semiconductor region in a region in which said first and second semiconductor regions form a junction is shallower than that of said semiconductor region in a region in which said semiconductor substrate and said first semiconductor region form a junction.

10. A semiconductor integrated circuit device according to claim 8, wherein each of said plurality of first connection holes is equal to and smaller than a connection hole arranged with a minimum pitch of the circuit in diameter.

Sub a3

11. A semiconductor integrated circuit device comprising:

a plurality of first connection holes for electrically connecting a first wire and a first semiconductor region formed in a first region of a primary face of a semiconductor substrate, to each other therethrough; and

a plurality of second holes for electrically connecting a second wire and a second semiconductor region formed in a second region of the primary face of the semiconductor substrate, to each other

therethrough, wherein each of said plurality of first connection holes is spaced from each other so that a pitch between the adjacent first connection holes is greater than a minimum pitch between connection holes of the circuit, and wherein each of said plurality of second connection holes is spaced from each other so that a pitch between the adjacent second connection holes are about equal to the minimum pitch of the connection holes of the circuit.

12. A method of manufacturing a semiconductor integrated circuit device comprising:

(a) a step of forming a semiconductor region of a first electrically conducting type in a first region on a primary face of a semiconductor substrate of a first electrically conducting type, and then forming, on said semiconductor substrate located in a top portion of the semiconductor region of said first electrically conducting type, a semiconductor region of a second electrically conducting type that has a greater area of a planar pattern than the semiconductor region of said first electrically conducting type, and thereby forming a zener diode composed of the semiconductor region of said first electrically conducting type and the semiconductor region of said second electrically conducting type;

(b) a step of forming an insulation film on the

primary face of said semiconductor substrate, and then forming a plurality of connection holes in said insulation film at an upper part of a region being outside a junction formed between the semiconductor regions of said first and second electrically conducting types; and

(c) a step of forming a wire at the upper part of said insulation film, and thereby electrically connecting said wire and the semiconductor region of said second electrically conducting type through said plurality of connection holes.

13. A method of manufacturing a semiconductor integrated circuit device according to claim 12, wherein the semiconductor region of said second electrically conducting type that constitutes a part of said zener diode is formed simultaneously in a step of forming a semiconductor region of a second electrically conducting type for providing configures a source and a drain of a MISFET in a second region on the primary face of the semiconductor region of said first electrically conducting type.

14. A method of manufacturing a semiconductor integrated circuit device according to claim 12, wherein each of said plurality of connection holes is spaced from each other so that a pitch between the

adjacent connection holes is greater than a minimum pitch between connection holes of the circuit.

15. A semiconductor integrated circuit device comprising:

a first semiconductor region of a first electrically conducting type formed in a primary face of a semiconductor substrate;

a second semiconductor region of a first electrically conducting type formed on said semiconductor substrate at an upper part of said first semiconductor region, the second semiconductor region having higher impurity concentration than said first semiconductor region;

a third semiconductor region of a second electrically conducting type formed in said semiconductor substrate at upper parts of said first and second semiconductor regions;

a first insulation film formed on the primary face of said semiconductor substrate;

a first connection hole that consists of a plurality of connection holes formed in said first insulation film at the upper part of said first semiconductor region; and

a second connection hole that consists of a plurality of connection holes formed in said first insulation film at the upper part of said third

semiconductor region, wherein said second connection hole is formed in an upper part of a region in which said first semiconductor region and said third semiconductor region form a junction.

16. A semiconductor integrated circuit device according to claim 15, wherein first and second electrically conductive connection bodies are provided inside said first and second connection holes, and wherein a first wire connected to said first semiconductor region via said first electrically conductive connection body, and a second wire connected to said third semiconductor region via said second electrically connecting connection body are formed at an upper part of said first insulation film.

17. A semiconductor integrated circuit device according to claim 16, wherein said first semiconductor region is composed of a fourth semiconductor region of a first electrically conducting type, and a fifth semiconductor region connected to said first electrically conductive connecting body via said fourth semiconductor region, the fifth semiconductor region being lower than said fourth semiconductor region in impurity concentration.

18. A semiconductor integrated circuit device

according to claim 15, wherein said first and second connection holes are formed by using a photo-resist film as a mask and by dry etching said first insulation film.

19. A semiconductor integrated circuit device comprising:

a first semiconductor region formed in the primary face of a semiconductor substrate;

a second semiconductor region of a first electrically conducting type formed on said semiconductor substrate at an upper part of said first semiconductor region;

a third semiconductor region of a second electrically conducting type formed on said semiconductor substrate at upper parts of said first and second semiconductor regions;

a first insulation film formed on the primary face of said semiconductor substrate;

a first connection hole composed of a plurality of connection holes formed on said first insulation film at the upper part of said first semiconductor substrate; and

a second connection hole composed of a plurality of connection holes formed on said first insulation film at an upper part of said third semiconductor region, wherein a minimum pitch between the adjacent connection holes of said second connection hole is greater than

that between the adjacent connection holes of said first connection hole.

20. A semiconductor integrated circuit device according to claim 19, wherein said first semiconductor region is a semiconductor region of a second electrically conducting type and is lower than said second semiconductor region in impurity concentration.

21. A semiconductor integrated circuit device according to claim 19, wherein said first semiconductor region is a semiconductor region of a second electrically conducting type that configures a collector region of a bipolar transistor, said second semiconductor region is a semiconductor region of a first electrically conducting type that configure a base region of said bipolar transistor, and said third semiconductor region is a semiconductor region of a second electrically conducting type that constitutes an emitter region of said bipolar transistor.

add A6

add B4

add C10